

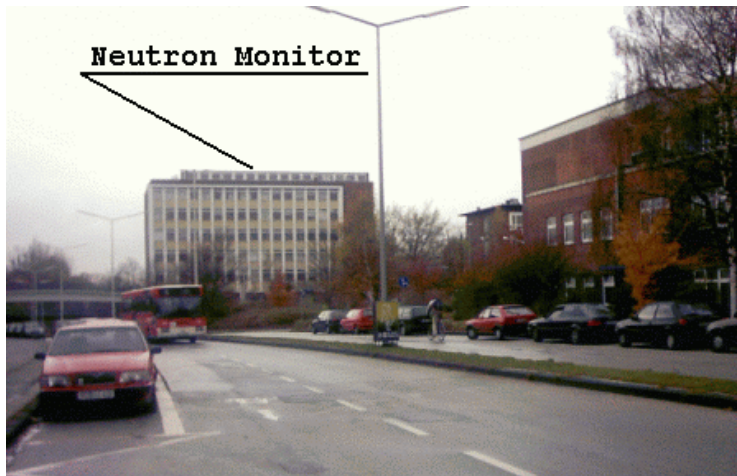
# Upgrading the Kiel Neutron Monitor

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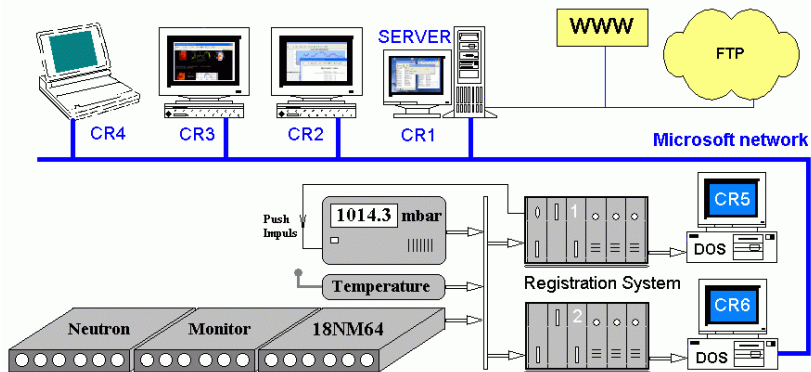
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Solar Extreme Events 2007 Symposium  
Neutron Monitor Workshop  
Athens, Greece, September 24–27

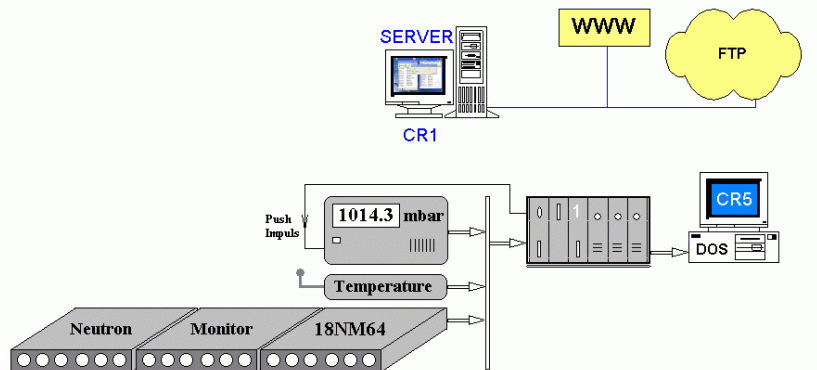
# Kiel 18NM24 Neutron Monitor (running since 1957)



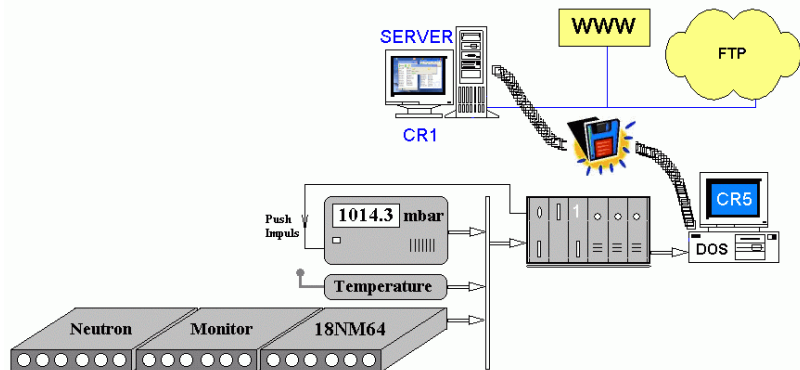
# Original 1990s IZMIRAN registration system



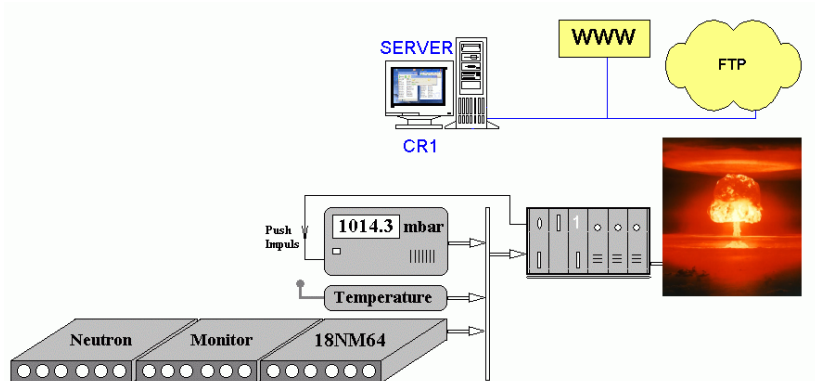
# Registration system's redundancy is lost



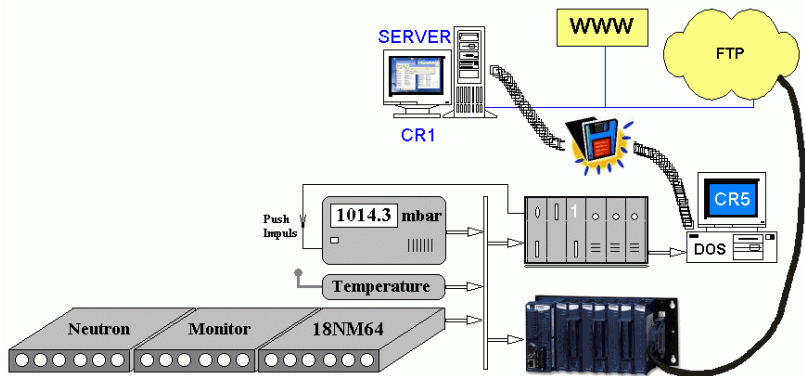
# Data transfer via "sneaker network"



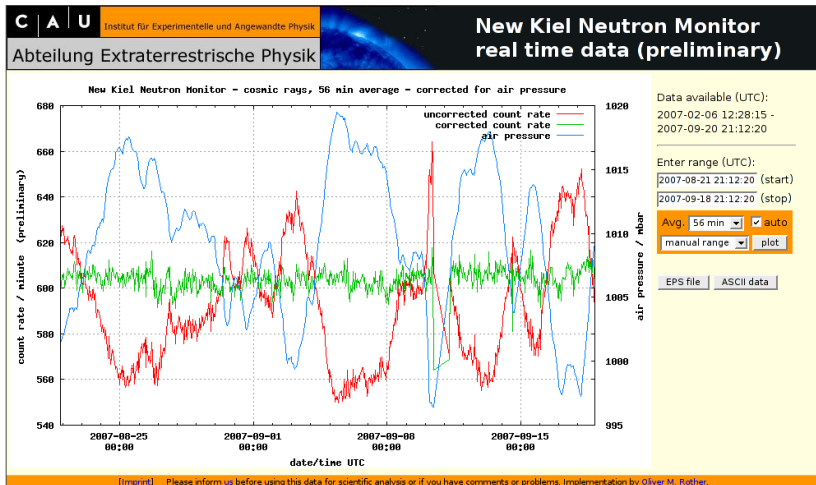
# Imminent fatal failure at any time



# New 2006's registration system: NI CompactFieldPoint



# New 2006's registration system: NI CompactFieldPoint





# New 2006's registration system: NI CompactFieldPoint

## Problems:

- high hardware and software costs, several thousands EUR
- programming language LabView: suited for small, quickly programmed data registration and control applications, **not** for complex systems (badly maintainable code)
- realtime glitches, e.g. loses counts during ftp data transfer of archive files
- proprietary: support depends on commercial supplier, source code and schematics not available – not suited for long-term applications

# Registration system requirements

What do we need?

- (sub)microsecond resolution
- short (zero) deadtimes
- optional recognition of PWM signals and multiplicities
- low power consumption
- redundancy
- long-term availability of parts
- cost-efficiency

# Does such kind of device exist?

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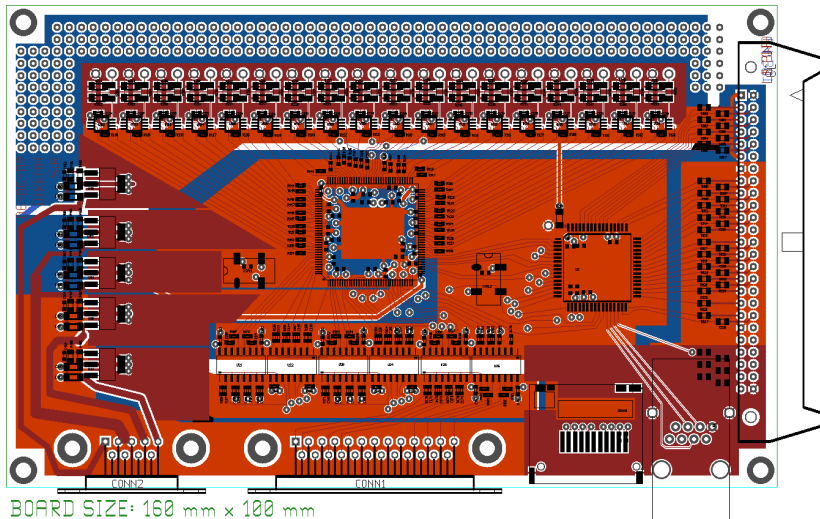
# Does such kind of device exist?

Yes!

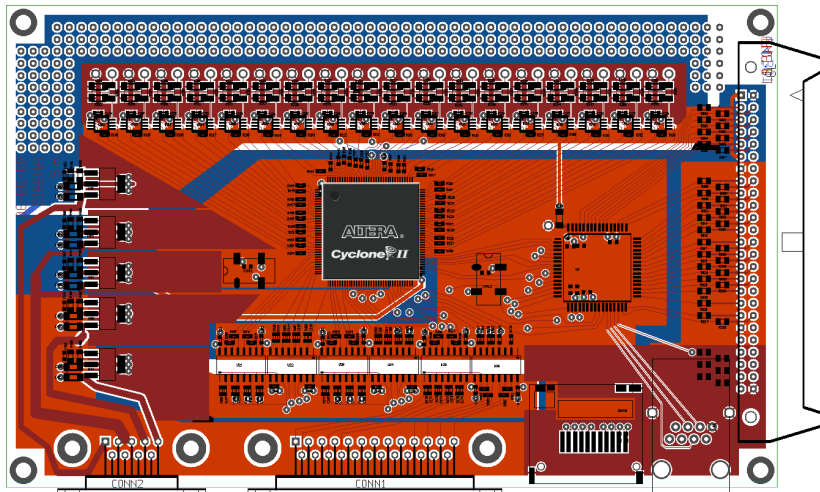
# Solution: Eierlegende Wollmilchsau



# The KiNeMoNIC registration board (DIRENA based)

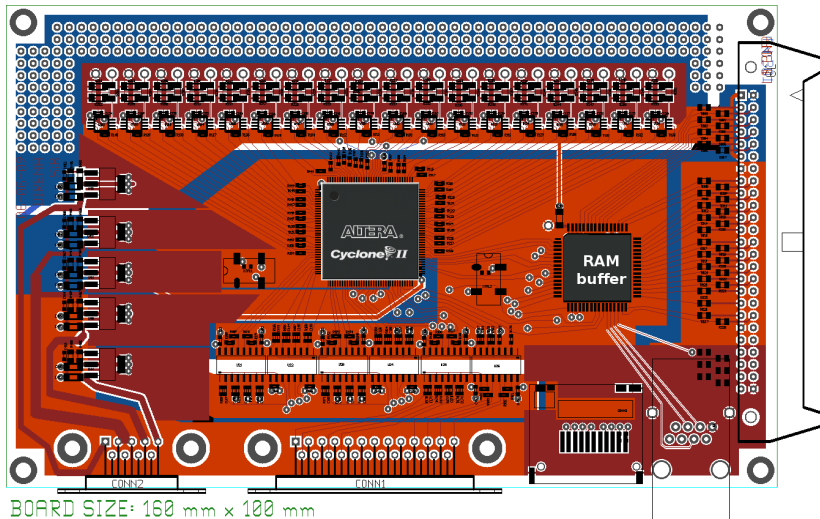


# The core: Altera Cyclone II FPGA @ 20–200 MHz



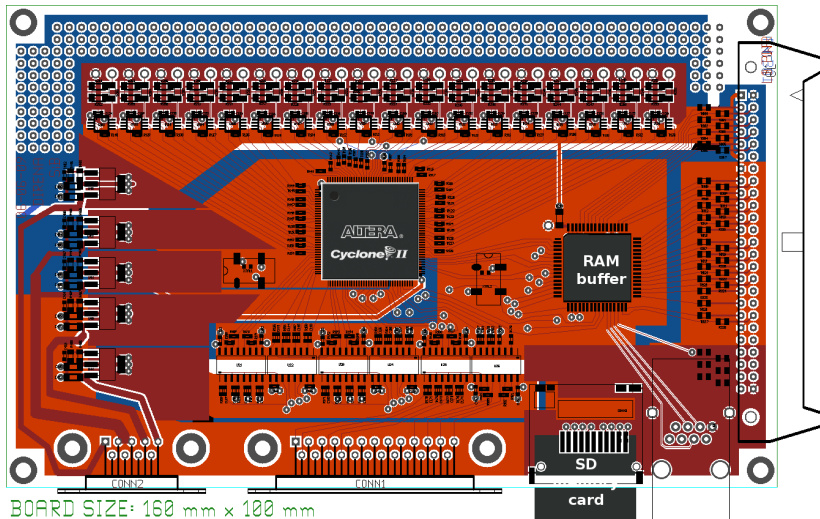
BOARD SIZE: 160 mm x 100 mm

# KiNeMoNIC's data storage system

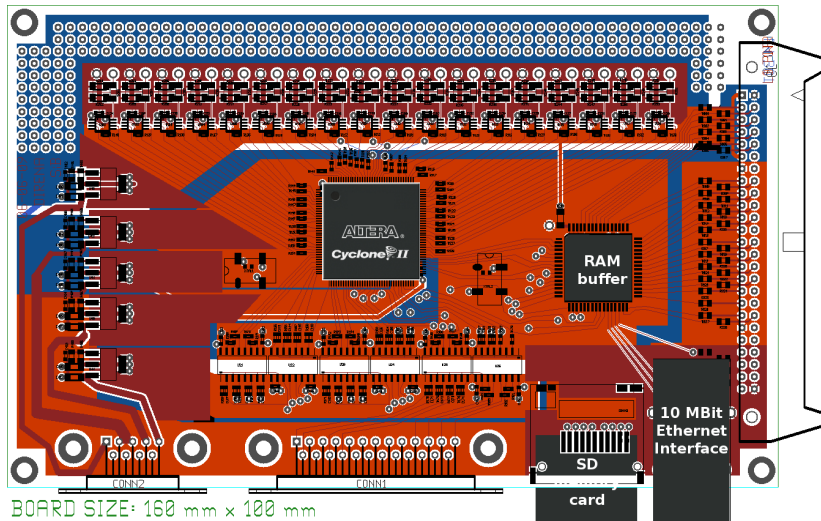




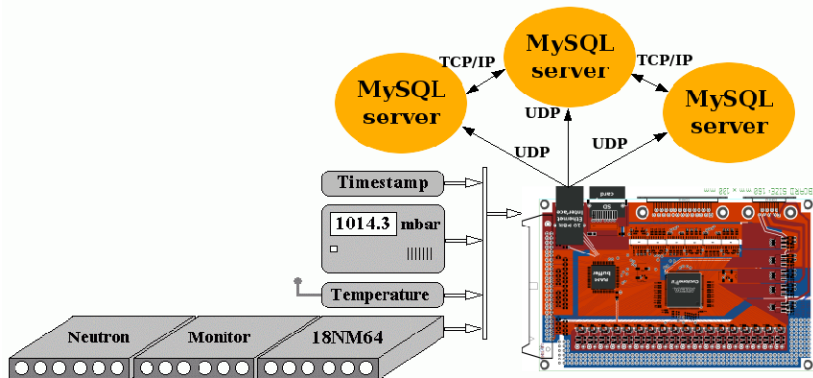
# KiNeMoNIC's data storage system



# Data distribution



# The KiNeMoNIC registration system



# Conclusion

## KiNeMoNIC – Kiel Neutron Monitor Network Interface Controller

- NM count rate to UDP packet converter
- proved maturity on MSL project (Mars Science Lab)
- purely hardware based
- low power consumption
- (sub)microsecond resolution, zero deadtime
- cost-efficient (about EUR 200 including PCB)
- FPGA code, pcb schematics and layouts are planned to be available under GPL (GNU Public License)